THRESHOLD VOLTAGE ROLL-OFF COMPENSATION USING BACK-GATED MOSFET DEVICES FOR SYSTEM HIGH-PERFORMANCE AND LOW STANDBY POWER

DESCRIPTION

Field of the Invention

[0001] The present invention relates to complementary metal oxide semiconductor (CMOS) devices, and more particularly to an integrated circuit (IC) that includes metal oxide semiconductor field effect transistors (MOSFETs) in which the back-gates or body nodes of the MOSFETs are 'statically' biased to obtain system high-performance, while maintaining low system standby power.

Background of the Invention

[0002] Clock gating is used in high performance semiconductor systems to reduce average active power by idling functional units and preventing wasteful events. This is disclosed, for example, in the article to N. Kurd, et al. entitled Multi-GHz Clocking Scheme for Intel® Pentium® 4 Microprocessor", ISSCC Digest of Technical Papers, 2001, p. 404. However, with technology scaling, leakage power of idle units becomes a large fraction of the total chip power. As a result, the overall power savings achievable by clock gating alone is diminishing.

[0003] Dynamic MOSFET threshold voltage (Vt) control schemes to meet the opposing requirements of high-performance, during system functional units active periods, and low power, during system functional units idle periods, have been proposed. See, for example, co-assigned and co-pending U.S. Application Serial No. 10/639,942, filed August 13, 2003, entitled "Device Threshold Control of Front-Gate Silicon-On-Insulator MOSFET using a Self-Aligned Back-Gate"; and the article to J. Tschang, et al.,

entitled "Dynamic-Sleep Transistor and Body Bias for Active Leakage Power Control of Microprocessors", ISSCC Digest of Technical Papers, 2003, p. 102.

[0004] In these prior art schemes, back-gated (SOI technology) or body node (bulk technology) MOSFETs are employed. By applying the proper bias to the nMOSFET back-gate or body node, its threshold voltage can be dynamically changed from low values (≤ 0 Volts), during system active periods for maximum performance, to high values (≥ 0.2 Volts) during system idle periods for minimum leakage power. For pMOSFETs, the opposite voltages are applicable.

[0005] The overall performance impact of these dynamic leakage control techniques on the system is dictated by the time required to switch the transistor back-gate or body node voltage during "idle" or "active" transitions. This time can be as large as several clock cycles. Also, for any of these dynamic leakage control techniques, to achieve reduction in the overall power, the leakage energy saved during the "idle" period must be larger than any energy overhead incurred during switching the transistor back-gates or body nodes between "idle" and "active" modes. The minimum "idle" time required to achieve overall power saving is dictated by the energy spent in switching the back-gate or body nodes and may account to several additional clock cycles.

[0006] It is an object of the present invention to provide a methodology in which the back-gates or body nodes of MOSFETs in a system or chip can be 'statically' biased for high performance and low standby power.

Summary of the Invention

[0007] In view of the aforementioned objective, the present invention provides a method whereby the back-gates or body nodes of MOSFETs in a system or chip are 'statically' biased to obtain a high performance system or chip, while maintaining low system or chip standby power. In particular, a method is provided in which the static

bias of a nominal MOSFET comprising either a back-gate or a body node is first determined and thereafter the determined static bias is introduced on the system or chip. The term "nominal" is used throughout the present application to indicate that all device parameters such as, for example, channel length, and gate oxide thickness, assume their average or mean values for a particular technology. For example, in current technology, the nominal channel length, L_{nom}, is 25 nm. However, due to process variations, the channel length of current MOSFETs can have a nominal maximum length, L_{max}, of 32.5 nm, and a nominal minimum channel length, L_{min}, of 17.5 nm.

[0008] For devices in which the channel length is L_{nom}, the threshold voltage, Vt, is equal to Vt_{nom} and the off-current, I-off is also equal to $I\text{-}off_{nom}$. For devices in which the channel length is L_{max}, the threshold voltage is equal to Vt_{max} and the off-current is equal to $I\text{-}off_{min}$. For devices in which the channel length is L_{min}, the threshold voltage is equal to Vt_{min} and the off-current is equal to $I\text{-}off_{max}$.

[0009] Transistors that have a channel length above nominal are referred to herein as long channel devices, whereas transistors that have a channel length less than nominal are referred to herein as short channel devices. The longer channel devices typically have a higher threshold voltage and lower off-current than shorter channel devices.

[0010] The method of the present invention is based on the use of the back-gate or body node bias to compensate MOSFET threshold voltage roll-off. The term threshold voltage (i.e., Vt) roll-off is used herein to denote the different device threshold voltages that can exist within a system or chip caused by process variations that effect the channel length of each transistor.

[0011] In the present invention, a semiconductor system or chip having a plurality of transistors is designed with the channel length of L_{nom}. In accordance with the present invention, it is assumed that the channel length of these transistors at the completion of chip manufacturing is L_{max}. This enables one to set the off-current to the maximum

value of I-off_{max} which is done by setting the threshold voltage value to Vt_{min}. The Vt_{min} for these transistors is obtained during processing by using the proper implant dose. After manufacturing, the transistors are then tested to determine the off-current thereof. Some transistors within the system or chip will have an off-current value that meets a current specification. For those transistor devices, no further compensation is required. For other transistors within the system or chip, the off-current is not within the predetermined specification. For those transistors, threshold voltage roll-off has occurred since they are transistors that have a channel length that is less than nominal. For such short channel transistors, the threshold voltage is low, even lower than Vt_{min}, and the off-current is high, even higher than I-off_{max}. Compensation of the short channel transistors is achieved in the present invention by biasing the back-gate or body node to give increased threshold voltage that is about equal to Vt_{min} and hence an off-current that meets the predetermined specification, which is about equal to I-off_{max}.

[0012] In broad terms, the method of the present invention comprises the steps of:

[0013] designing a semiconductor chip or system having a plurality of transistor devices in which the channel length of each transistor device is equal to L_{nom};

[0014] setting off-current of each transistor device to I-off_{max} by predeterming that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor such that threshold voltage is equal to Vt_{min};

[0015] testing the off-current of each transistor device; and

[0016] biasing the back-gate or the body nodes of some transistor devices that have an off-current that does not meet a preselected specification of about I-off_{max} to increase the threshold voltage to about Vt_{min} thereof thereby compensating threshold voltage roll-off within said semiconductor chip or system.

[0017] In the present invention, the threshold voltage of each transistor device present in the chip or system is set assuming that each transistor has its nominal maximum value of channel length. The threshold voltage of each transistor device is thus set to an off-current that meets a preselected specification of I-off_{max} . In this step of the present invention, the threshold voltage of the transistor devices is set by implanting into the channel region of the transistor devices. The degree of threshold voltage setting can be controlled by preselecting the implant conditions and ion dosage used.

[0018] After setting the threshold voltage of each transistor device within the chip or system to Vt_{min}, the threshold voltage of each transistor device can be measured after manufacturing. Some transistors will not need any further adjusting, others will require additional adjusting. The additional adjusting is performed by biasing the back-gate or the body node (i.e., well region) of the transistor. The biasing occurs after manufacturing of the semiconductor chip or system during testing thereof or it can be done at a later time.

[0019] Biasing may be achieved by an external DC voltage source, an internal circuit that can deliver a potential to the back-gate or the body node of the second transistors or by an external clock system that can deliver a potential.

Brief Description of the Drawings

[0020] FIG. 1 is a graph of threshold voltage roll-off Vt @ V_{DS}= 1 volt (Volt) vs. channel length (nm) for a nominal double-gated MOSFET device.

[0021] FIG. 2 is a graph showing the nominal device off-current (nA/μm) vs. channel length (nm).

Detailed Description of the Invention

[0022] The present invention, which provides a method for statically biasing the back-gates or the body nodes of MOSFETs to obtain system high performance, while maintaining low system standby power, will now be described with reference to the drawings that accompany the present application. The drawings represent one possible implementation of the present invention.

[0023] As indicated above, the present invention provides a method for statically biasing the back-gates or the body nodes of MOSFETs to obtain system high performance, while maintaining low system standby power. The inventive method is based on the use of the back-gate or the body node of an MOSFET to compensate MOSFET device threshold roll-off which is caused by variations in device parameters during fabrication of the transistors. The inventive methodology is based on adjusting the threshold voltage during processing by first assuming that each transistor has its nominal maximum channel length and implanting into the channel region of each transistor. After manufacturing, additional adjustments in threshold voltage is made to those devices not meeting a pre-selected off-current value by biasing the back-gates or the body nodes of those transistors.

[0024] The inventive method of threshold voltage compensation begins with first designing a semiconductor chip or semiconductor system that includes a plurality of transistor devices that have a channel length equal to the nominal channel length value. The transistor devices formed in the present invention are either back-gate devices or devices that include a body node (i.e., n-well or p-well). The transistors are typically MOSFETs that include a gate conductor, at least one gate dielectric, and a channel region located beneath the gate conductor.

[0025] The back-gate devices are formed utilizing techniques well known to those skilled in the art. One such process of forming a back-gated device is disclosed, for

example, in U.S. Patent Application Serial No. 10/639,942, filed August 13, 2002, the contents of which are incorporated herein by reference. Back-gate devices are typically characterized as MOSFET devices having a front gate and a back gate that are separated from a Si channel by gate dielectrics.

[0026] The devices containing body nodes are formed utilizing conventional complementary metal oxide semiconductor (CMOS) processing schemes that are well known to those skilled in the art. The body node devices are generally characterized as a bulk MOSFET device in which the substrate node can be biased to adjust the device threshold.

[0027] In typical transistor devices, the channel length ranges in value from a nominal minimum value to a nominal maximum value. This variation in channel length is due to process variations that exist during the fabrication of each transistor. The nominal value of transistor channel length, L_{nom}, is based on the technology being used. For today's technology, the nominal channel length is 25 nm. Because of process variations however, the transistors have a channel length that can vary from 17.5 nm (nominal minimum) to 32.5 nm (nominal maximum). Those transistors that have channel lengths above nominal are referred to long channel devices, while the transistors that have channel lengths less than nominal are referred to as short channel devices.

[0028] As known to those skilled in the art, the threshold voltage of longer channel devices is typically greater than the threshold voltage of shorter channel devices. As a consequence, the longer channel devices have a lower off-current than the off-current of shorter channel devices. Consequently, a methodology is needed to compensation for the variation in threshold voltage that can exists in a semiconductor chip or system.

[0029] During the manufacturing of the semiconductor chip or system, the threshold voltage of the transistor devices is compensated (i.e., adjusted) by first assuming that each transistor device has its nominal maximum channel length and then implanting into

the channel region such that each transistor device has substantially the same threshold voltage of about Vt_{min} and an off-current that meets a preselected specification of about I-off_{max}.

[0030] The exact values of the threshold voltage achieved after this compensation step may vary from semiconductor chip to semiconductor chip. Typically, however, the threshold voltage that is achieved after the compensating step is from about 50 to about 450 millivolts, with a threshold voltage from about 100 to about 150 millivolts being more typical.

[0031] Likewise, the off-current achieved after the compensating step may vary from semiconductor chip to semiconductor chip. Typical values of off-current that can be achieved after the compensating step are from about 50 to about 150 nA/μm, with an off-current after compensation of about 100 nA/μm being more typical. Although these ranges for off-current are specifically provided, the present invention can be used to achieve any preselected off-current that may be required.

[0032] In this step of the present invention, the threshold voltage of any long channel devices would be compensated by lower the threshold voltage of those transistors such that the long channel devices have a threshold voltage that is substantially equal to the threshold voltage of the short channel devices. During this step of the present invention in which the threshold voltage of any long channel devices is lowered, the off-current of those transistor devices is also increased to a value that substantially matches that of the short channel devices.

[0033] The threshold voltage of the transistor devices is compensated by implanting either an n-or p-type dopant into the channel region of each device. Suitable n-type dopants that can be employed in the present invention include, but are not limited to Group V dopants such as, for example, As, Sb, and/or P, while suitable p-type dopants that are employed in the present invention include Group III dopants such as B.

[0034] The degree of compensation can be controlled by preselecting the implant conditions and the ion dosage used in this embodiment of the present invention. The implant conditions employed in the present may vary over wide ranges and are dependent upon the ion that is being implanted and the degree of threshold voltage adjustment needed. Typical implant conditions that can be used in the present invention are as follows: implanting at an energy from about 5 to about 30 keV.

[0035] The ion dosage that can be employed in the present invention may vary depending upon the degree of compensation required as well as the type of ion that is being implanted into the channel region of the longer channel devices. For example, when p-type dopants are employed the ion dosage employed in the present invention can be from about 1E11 to about 1E13 atoms/cm^2. When n-type dopants are employed, the ion dosage is typically from about 1E11 to about 1E13 atoms/cm^2.

[0036] After the first compensation step, and at a time after manufacturing, the threshold voltage of the transistor devices requiring further adjusting can be made, during or after testing, by biasing the back-gate or the body node thereof. The biasing increases the threshold voltage of shorter channel devices to a value such that the off-current thereof also increases.

[0037] In this step of the present invention, the biasing of the back-gates or body nodes may be achieved by an external DC voltage source, an internal circuit that can deliver a potential to the back-gate or the body node of the second transistors or by an external clock system that can deliver a potential.

[0038] When an external clock system is used in this step of the present invention, the biasing can be achieved by comparing the system clock to the output of an on-chip running oscillator. The use of the external clock has the advantage of a temperature self-adjusting back bias voltage.

[0039] The above description provides an overview of the method of the present invention. The following description, which makes reference to FIGS. 1 and 2, provide one application of the method of the present invention for a NMOS transistor having a halo design.

[0040] Reference is made to FIG. 1 which is a graph of threshold voltage roll-off Vt @ V_{DS}= 1 volt (Volt) vs. channel length (nm) for a nominal double-gated MOSFET device. In FIG. 1, Curve A denotes the Vt roll-off for a nominal double-gate MOSFET device with, as an example, a channel length L_{chan} = 25 nm (±7.5 nm), a front gate with $T_{inv,FG}$ = 1.5 nm, a back gate with $T_{inv,BG}$ = to 3.0 nm and a silicon thickness T_{Si} = 10 nm. Curve B and Curve C of FIG. 1 show the worst and best case Vt roll-off due to a ± 3 sigma variations in various process parameters such as source/drain junction depth, gate oxide thickness, channel implant dose and energy, halo implant dose and energy, and doping fluctuations. Note that as the channel length decreases, the variation in the device threshold increases since the variations in the process parameters have a more pronounced impact on the smaller channel length devices. CURVE X of FIG. 2 shows the worst case process device off-current as a function of channel length that corresponds to the Vt roll-off characteristics shown in Curve B of FIG. 1. Curve Y of FIG. 2 shows, as an example, that the off-current of the minimum channel device, L_{chan} = 17.5 nm, is 350 nA/μm at V_{DS} = 1 Volts. For the following discussion, assume that the required maximum device off-current is I-off_{max} (~ 350 nA/μm at V_{DS} = 1 Volts) including all device variations such as: gate oxide thickness, channel implant and halo implant doses, doping fluctuations, ...etc. To meet this requirement, the following techniques can be used:

1) First, using proper channel implant dose, the threshold voltage of the longer channel devices are adjusted (L_{chan} = 32.5 nm) to obtain the required off-current I-off_{max} as shown in Curve D of FIG. 1 and Curve X of FIG. 2.

2) second, adjusting the back-gate bias for only the shorter devices (L_{chan} < 32.5 nm) to increase their threshold voltage as shown in Curve D of FIG. 1. The threshold voltage

shift Δ shown in FIG. 1 is chosen such that I-off$_{min}$ (Curve Y of FIG. 2) is equal I-off$_{max}$ under worst case device variations condition. This back-gate bias can be supplied externally or generated on chip by comparing the system clock to the output of an on-chip free running oscillator. The later case has the advantage of a temperature self adjusting back-bias voltage.

[0041] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.